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10/772,434	02/06/2004	Ramachandran Krishnaswamy	333772000800	5995

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MORRISON & FOERSTER LLP
425 MARKET STREET
SAN FRANCISCO, CA 94105-2482

EXAMINER	
LO, SUZANNE	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/772,434	KRISHNASWAMY ET AL.	
	Examiner	Art Unit	
	Suzanne Lo	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/25/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 have been presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. **Claims 1-3, 5-6, 8-16, 19-23 are rejected** under 35 U.S.C. 103(a) as being unpatentable over **Hollander (U.S. Patent Application Publication 2002/0073375 A1) in view of Botala et al. (U.S. Patent No. 6,868,513B1).**

As per claim 1, Hollander is directed to a method for developing a test program in general purpose C/C++ constructs, the test program for testing a semiconductor integrated circuit (IC) in a

semiconductor test system **([0040]-[0041])**, the method comprising: describing test system resources, test system configuration, and module configuration in general-purpose C/C++ constructs for the development of a test program to test the IC on the semiconductor test system **([0035], [0042]),** wherein describing test system configuration comprises specifying a site controller for controlling at least one test module **(Figure 1, test files 12, 20, and drive 32)**; describing a test sequence in general-purpose C/C++ constructs for the development of the test program to test the IC on the semiconductor test system **([0043])**; describing a test plan in general-purpose C/C++ constructs for the development of the test program to test the IC on the semiconductor test system **([0044])**; describing test conditions in general-purpose C/C++ constructs for the development of the test program to test the IC on the semiconductor test system **([0045])**; describing test patterns in general-purpose C/C++ constructs for the development of the test program to test the IC on the semiconductor test system **([0068])**; and describing timing of the test patterns in general-purpose C/C++ constructs for the development of the test program to test the IC on the semiconductor test system **([0060], [0068], [0085])**; *and storing the test program in memory of the semiconductor test system* **([0269])** but fails to explicitly disclose wherein each test module includes vendor-supplied hardware and software components for applying a test to the IC, *wherein each vendor-specific software module comprises a module-specific compiler for generating test pattern objects.*

Botala teaches a test module which includes vendor-supplied hardware and software components for applying a test to a DUT **(column 1, lines 30-37)** *wherein each vendor-specific software module comprises a module-specific compiler for generating test pattern objects* **(column 7, line 4 – column 8, line 3 and Multi-DUT test program 14, Figure 1)**. Hollander and Botala are analogous because they are both from the same field of endeavor, developing a test program. It would have been obvious at the time of the invention to an ordinary person skilled in the art to combine the method of developing a test program of Hollander with the vendor supplied components in order to drastically reduce test time and

cost while significantly increasing throughput of the existing installed tester base **(Botala, column 1, lines 17-19)**.

As per claim 2, the combination of Hollander and Botala already discloses the method of claim 1, wherein describing test system resources comprises: specifying a resource type, wherein the resource type is associated with at least one test module for applying a test to the IC; specifying a parameter type associated with the resource type, and specifying a parameter of the parameter type **(Hollander, [0068]-[0070])**.

As per claim 3, the combination of Hollander and Botala already discloses the method of claim 1, wherein describing test system configuration comprises: specifying an input port of a module connection enabler, wherein the test system couples the site controller to the module connection enabler at the input port, and the module connection enabler couples the site controller to the at least one test module **(Hollander, Figure 1, test files 12, 20 and drive 32)**.

As per claim 5, the combination of Hollander and Botala already discloses the method of claim 1, wherein describing module configuration comprises: specifying a module identifier for specifying a module type **(Hollander, [0074]-[0076])**; specifying executable code for controlling *the* test module of the module type specified by the module identifier **(Hollander, [0074]-[0076])**; and specifying a resource type *and resource units* associated with the test module **(Hollander, [0068]-[0070])**.

As per claim 6, the combination of Hollander and Botala already discloses the method of claim 5, the method further comprising specifying a slot identifier for specifying an output port of a module connection enabler, wherein the test system couples the test module to the module connection enabler at the output port, and the module connection enabler couples the test module to a corresponding site controller **(Hollander, [0074]-[0076])**.

As per claim 8, although Hollander and Botala do not explicitly disclose the method of claim 5, wherein the executable code is a dynamic link library, it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to minimize memory usage.

As per claim 9, the combination of Hollander and Botala already discloses the method of claim 5, further comprising specifying a vendor identifier for identifying the provider of the test module **(Hollander, Figure 3)**.

As per claim 10, the combination of Hollander and Botala already discloses the method of claim 5, further comprising specifying an identifier of the maximum number of resource units available in connection with the resource type **(Hollander, Figure 3)**.

As per claim 11, although Hollander and Botala do not explicitly disclose the method of claim 5, wherein the resource type is digital tester pins and the resource units are tester channels, Hollander discloses driving any simulator signals **([0095])** and resource units as tester channels **(Figure 1, drive 32, test generator 26)** so it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to implement a comprehensive testbench.

As per claim 12, although Hollander and Botala do not explicitly disclose the method of claim 5, wherein the resource type is analog tester pins and the resource units are tester channels, Hollander discloses driving any simulator signals **([0095])** and resource units as tester channels **(Figure 1, drive 32, test generator 26)** so it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to implement a comprehensive testbench.

As per claim 13, although Hollander and Botala do not explicitly disclose the method of claim 5, wherein the resource type is RF tester pins and the resource units are tester channels, Hollander discloses driving any simulator signals **([0095])** and resource units as tester channels **(Figure 1, drive 32, test generator 26)** so it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to implement a comprehensive testbench.

As per claim 14, although Hollander and Botala do not explicitly disclose the method of claim 5, wherein the resource type is power supply pins and the resource units are tester channels, Hollander discloses driving any simulator signals **([0095])** and resource units as tester channels **(Figure 1, drive 32, test generator 26)** so it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to implement a comprehensive testbench.

As per claim 15, although Hollander and Botala do not explicitly disclose the method of claim 5, wherein the resource type is digitizer pins and the resource units are tester channels, Hollander discloses driving any simulator signals **([0095])** and resource units as tester channels **(Figure 1, drive 32, test generator 26)** so it would have been obvious to one of ordinary skill in the art at the time of the invention to include the above limitation in order to implement a comprehensive testbench.

As per claim 16, the combination of Hollander and Botala already discloses the method of claim 5, wherein the resource type is arbitrary waveform generation pins and the resource units are tester channels **(Hollander, [0095], Figure 1, Drive 32, test generator 26)**.

As per claim 19, the combination of Hollander and Botala already discloses the method of claim 1, wherein describing test conditions comprises: specifying at least one test condition group **(Hollander, Figure 1, test files 20 and Figure 2, test files 205)**.

As per claim 20, the combination of Hollander and Botala already discloses the method of claim 19, wherein describing test conditions further comprises: specifying at least one specification set including at least one variable; and specifying a selector for selecting an expression to be bound to a variable **(Hollander, Figure 1, test files 20 and Figure 2, test files 205)**.

As per claim 21, the combination of Hollander and Botala already discloses the method of claim 20, wherein association of the test condition group with a selector for the at least one specification set defines a test condition **(Hollander, Figure 1, test files 20 and Figure 2, test files 205)**.

As per claim 22, the combination of Hollander and Botala already discloses the method of claim 21, wherein the test condition is an object **(Hollander, Figure 1, test files 20 and Figure 2, test files 205)**.

As per claim 23, the combination of Hollander and Botala already discloses the method of claim 1, wherein describing a test sequence comprises specifying: a result of executing a flow or test; an action based upon the result; and a transition to another flow or test based upon the result **(Hollander, Figure 1, module 24)**.

3. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollander (U.S. Patent Application Publication 2002/0073375 A1) and Botala et al. (U.S. Patent No. 6,868,513B1) **in further view of National Instruments ("Matrix Switch Expansion Guide").**

As per claim 4, the combination of Hollander and Botala is directed to the method of claim 3, but fails to specifically disclose wherein the module connection enabler is a switch matrix. National Instruments teaches a switch matrix as a connection enabler for unit under test **(page 1, 1st paragraph)**. Hollander, Botala, and National Instruments are analogous art because they are both from the same field of endeavor, testing circuit designs. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the test program of Hollander and Botala with the switch matrix of National Instruments in order to eliminate the need to duplicate instruments and reduce the cost to test **(National Instruments, page 1, 1st paragraph)**.

As per claim 7, the combination of Hollander and Botala is directed to the method of claim 6, but fails to specifically disclose wherein the module connection enabler is a switch matrix. National Instruments teaches a switch matrix as a connection enabler for unit under test **(page 1, 1st paragraph)**. Hollander, Botala, and National Instruments are analogous art because they are both from the same field of endeavor, testing circuit designs. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the test program of Hollander and Botala with the switch matrix of

National Instruments in order to eliminate the need to duplicate instruments and reduce the cost to test **(National Instruments, page 1, 1st paragraph)**.

4. **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hollander (U.S. Patent Application Publication 2002/0073375 A1) and Botala et al. (U.S. Patent No. 6,868,513B1) **in further view of Schauss et al. (U.S. Patent No. 5,181,201).**

As per claim 17, the combination of Hollander and Botala is directed to the method of claim 5, but fails to specifically disclose wherein the resource type is associated with resource units, the method further comprising specifying an indicator relating to which resource units are disabled. Schauss teaches an indicator for disabled resource units **(column 13, lines 54-62)**. Hollander, Botala, and Schauss are analogous art because they are both from the same field of endeavor, interfacing chip devices. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the test program of Hollander and Botala with the disabled indicator of Schauss in order to track non-operational inputs **(Schauss, column 13, lines 54-62)**.

As per claim 18, the combination of Hollander, Botala, and Schauss already discloses the method of claim 17, wherein resource units indicated as disabled represent defective resource units of the test module **(Schauss, column 14, lines 13 - 24)**.

Response to Arguments

5. The 35 U.S.C. 101 rejection of claims 1-23 are withdrawn due to the amendment.

6. Applicant's arguments with respect to claims 1-23 have been considered but are unpersuasive.

7. In response to Applicant's argument that Hollander and Botola either individually or in combination do not disclose the limitation "wherein each vendor-specific software module comprises a

module-specific compiler for generating test pattern objects", the Applicant is directed to column 7, line 4 – column 8, line 3 of Botala, as well as the accompanying Figure 1, Multi-DUT test program 14.

8. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., integrating vendor-supplied hardware and software modules into an open system architecture using a standard module interface) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

9. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

1. U.S Patent No. 5,488,573 issued to Brown et al. on 01/30/96.

2. U.S. Patent No. 6,195,774 B1 issued to Jacobson on 02/27/01.

3. U.S. Patent No. 6,779,170 B1 issued to Montrym on 08/17/04.

4. "Towards a Standard for Embedded Core Test: An Example" published by Marinissen et al. on 09/30/99.

5. "Synthesizing Testability Features into a Design with the Synopsys Test Compiler" published by Zhang et al. on 05/16/95.

10. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suzanne Lo
Patent Examiner
Art Unit 2128

SL
08/02/07

KAMINI SHAH
SUPERVISORY PATENT EXAMINER